VARIOPRINT Powering your Performance

Capabilities

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Content

At a glance

Page 2

Markets

Page 2

Industry

- Sensor Devices
- Measuring & Control Applications
- Test Systems
- Engineering Applications

Aerospace & Defense

- Sensor Technology
- Civil Aviation Applications
- Satellite Navigation Systems
- Radio Systems

Medical

- Cardiac Pacemakers
- Diagnostic Devices
- Monitoring Applications

Hightech & Life Science

- Watch Industry
- Smart Health Devices
- \cdot Light Detection

Telecommunication

- Antenna Systems
- Server Applications

Mobility

- Driver Assistance Systems
- LED Lights
- Toll and Traffic Management Systems

Specifications

Page 3

Products

- High Frequency
- Flex/Rigid flex
- Metal back
- Multilayer and HDI
- Single- and Double-sided

Surfaces

- ENIG, ENEPIG, EPIG, DIG
- Immersion Silver
- Immersion Tin
- Electroplate Gold
- OSP
- Lead free HASL
- ٠DIG

Materials

- •6 FR4
- 2 High Speed FR4
- 3 High TG FR4
- 5 Polyimide Woven Glass
- 4 Polyimide flex
- •1 Large selection of HF substrates

Certifications

- ISO 9001
- · ISO 14001
- AS 9100
- ITAR certified

The stated values and tolerances for standard and special specifications are guide values and may vary depending on the choice of material, PCB design and layout. Values must be checked in detail by our engineering department. We will be pleased to advise you personally!

Plating	Standard	Special
Etching tolerance (in relation to copper layer thickness)	± 20 μm	± 10 μm
Maximum copper layer thickness (Cladding and plated copper)	210 µm	400 µm
High surface copper thickness can require multiple solder mask process iterations in order to ensure sufficient solder mask coverage on traces and trace-edges.		
Aspect Ratio depth: through hole Ø	12:1	15:1
Aspect Ratio depth: blind via Ø	1:1	1:1.3

Surface	Thickness	solderable	bondable	Solder life time
Electroless Nickel / Immersion Gold (ENIG)	Ni 3.0 – 7.0 µm Au 0.05 – 0.11 µm	Yes	Yes	12 Months
Chemical Palladium – Immersion Gold (ENEPIG)	Ni: 3.0 – 7.0 µm Pd 0.08 – 0.25 µm Au 0.03 – 0.08 µm	Yes	Yes	12 Months
Electroless Palladium – Reductive Gold (EPIG) (No Nickel surface – good for RF)	Pd 0.10 – 0.20 μm Au 0.10 – 0.20 μm	Yes	Yes	12 Months
Reductive (chemical) Gold	Ni 3.0 – 8.0 µm Au 0.40 – 0.60 µm	Yes	Yes	12 Months
Electroplate Bond Gold	Ni 3.0 – 7.0 μm Au 0.05 – 0.11 μm	Yes	Yes	12 Months
Lead free HASL	1 – 30 µm	Yes	No	12 Months
Immersion Tin	0.8 -1.10 µm	Yes	No	6 Months
Immersion Silver	0.15 – 0.45 µm	Yes	No	6 Months
OSP	0.25 – 0.50 µm	Yes	No	6 Months
Electroplate Hard Gold (Connector Gold)	Ni 3.0 – 8.0 µm Au 0.8 – 3.0 µm	Not	suitable for sc or bonding	2
Direct Immersion Gold (DIG)	Au 0.2 – 0.3 µm	Yes	No	6 Months

Production panel dimension	Standard
Usable area on smallest panel	265 x 419 mm
Usable area on middle size panel	420 x 569 mm
Usable area on large panel	490 x 569 mm
Maximum PCB dimension (single/double sided only)	569 x 1180 mm

Line/Space	Standard	Special
Inner layer (trace width/distance)	75 μm / 75 μm	50 μm / 50 μm
Outer layer (trace width/distance)	75 μm / 75 μm	50 μm / 50 μm
Please see also chapter Technology - Fine line		

Laser	Standard	Special
µVia ratio depth vs diameter	1:1	On request
µVia drill diameter	100–250 µm	50 – 100 µm
µVia pad diameter	300 µm	250 µm

Mechanics	Standard	Special
Minimum drill diameter	120 µm	75 µm
Misalignment 1 st tooling drill pattern	± 30 µm	± 20 μm
Misalignment 2 nd tooling drill pattern	± 100 µm	± 30 μm
Misalignment drill – conductor pattern	± 50 μm	± 50 μm
Drill depth: through hole Ø	8:1	14:1
Drill depth: blind hole Ø	1:1	1:1.3
Outline route (X – Y Axis) (depending on PCB dimension)	from ± 50 μm to ± 300 μm	from ± 50 μm to ± 200 μm
Misalignment routing – drill pattern	± 150 µm	± 50 μm
Misalignment routing – conductor	± 150 μm	± 50 μm
Misalignment scoring (30° Angle) to drilling		± 150 μm

Plugging	Standard	Special
Minimum diameter PTH	0.150 mm	On request
Maximum diameter PTH	1.0 mm	On request
Blind Via depth (IPC related)	0.5 mm class II	0.4 mm class III
Minimum PCB thickness	0.2 mm	On request
Maximum PCB thickness	4.0 mm	On request
Selective plugging	available on request	
Plugging paste	Tayio THP 100 DX1	

Solder mask and Surface protection	Standard	Special	
Minimum clearance Solder mask – conductor pattern	80 µm	50 µm	
Minimum solder mask bar between pads	80 µm	50 µm	
Minimum solder mask thickness over conductor edge	5–7 µm (accordi	5–7 μm (according to IPC-SM-840)	
Minimum distance between conductor pattern and assembly print	150 µm	100 µm	
Minimum symbol height of legend ink	800 µm	500 µm	
Minimum symbol width of legend ink	120 µm	100 µm	
Solder mask rigid PCB's Peters Elpemer SD 246		mer SD 2467	
Solder mask flex PCB's	Peters Elpemer SD 2463		
Printed coverlay and / or stiffener	available		
Serialization and traceability down to the individual PCB	yes barcode and data matrix available		

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Electrical inspection	Standard
By flying probe tester (company Atg)	100% of the boards are inspected
Impedance measurement single ended	yes
Impedance measurement differential	yes
Test parameter	Open: 10 V (1 Ω – 10 kΩ)
	Short: 250 V (100 kΩ – 10 MΩ)

Data format	Standard	Desired
Layout	Gerber, Extended Gerber HPGL, IPC 356	ODB++
Drilling and routing	Excellon I + II, Sieb & Meyer, Posalux	
Drawings	PDF, Post-Script, HPGL	

Engineering



Early collaboration with VARIOPRINT enhances the efficiency and quality of your PCB design and final product. Our experienced, process-oriented engineering team provides tailored advice specifically suited to your needs, supporting you in achieving optimal results for your PCB application.

Varioprint supports you with

Material Expertise: Guidance on material selection, leveraging our extensive materials data-base to address any material-related challenges.

Application-Specific Knowledge: Expertise in applications tailored to specific markets, including adherence to industry standards and specifications.

Design Validation: Verification services for stackup, preliminary Gerber data, and material selection.

PCB Design Guidelines: Comprehensive design rules to optimize PCB performance and reliability.

Holistic Recommendations: Advice covering all aspects of PCB development for the best possible outcome.

Targeted Pre-Studies: Custom Design of Experiments (DOEs) to tackle specific challenges early on.

Testing & Measurement Proficiency: Full range of testing and measurement capabilities to ensure quality and reliability.

PCB base material



Material specialties	
Quantic [®] Ticer	High Performance, thin-film embedded resistor copper foil. Allows, increasing performance and reducing form factor.
3 Authorized Distributor	Embedded capacitance material (ECM) increases usable board area by allowing for the removal of many, if not all, capacitors equal to or below 0.1 µF and their associated solder joints and vias.
Embedded Capacitance Material	

Fine line	
Current status at Varioprint	Standard: line / space 75 μm / 75 μm Special: line / space 50 μm / 50 μm Standard: via / pad 75 μm / 300 μm Special: via / pad 40 μm / 200 μm Thinnest base copper: 5 – 9 μm Thinnest base material: 25 μm, 12.5 μm in special cases Please note that achievable line space is depending on total copper thickness. (cladding and plating)

High-frequency	
Current status at Varioprint	 Fusion Bonding of PTFE material Intermittent etching for inner and outer layers Plasma etchback Modelling of high-frequency engineering materials Pre-compensation of high-frequency engineering structures Impedance analysis High-frequency measurement technology Processing of high-frequency technology circuits up to 200 GHz
Laser cavities	
Laser cutted cavities for mmIC pockets	
High Frequency Waveguide Waveguide connection integrated into the PCB	
Controlled side wall etching for special High Frequency applications	

Via technology	
Current status at Varioprint	 Stacked µVias Filled Vias up to aspect ratio of 1:1.3 Filled Vias up to fill grade of 98% Depending on via size and diameter Via in pad Via drill mechanically down to 75µm Dual laser drilling for reliable µvia connections
Via in pad with plated through holes	
Via in pad with blind Vias	
µVia filling on blind holes Variable fill grade Also available as via in pad	
µVia filling for buried blind vias Variable filling grade Also available as via in pad	
Through hole filling Copper Filled Through hole vias	

Plugging	
Current status at Varioprint	 Filling / plugging of Vias from 0.5 to 4.0mm PCB thickness Filling / plugging of blind Vias with aspect ratio of 1:1 Filling / plugging of special drilling diameters available on request Filling/plugging on order
Plated through holes	
Buried vias	

Thermal management	
Current status at Varioprint	 Boards on aluminum Boards on copper Integration of thermal vias Processing HEREQUIST semi-finished products Processing Laird material
µVia filling on blind holes variable fill grade Also available as via in pad Usable for thermal vias	

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